CMOS PROCESS COMPATIBLE, TUNABLE NEGATIVE DIFFERENTIAL RESISTANCE (NDR) DEVICE AND METHOD OF OPERATING SAME

RELATED APPLICATIONS

The present invention claims priority to and is a continuation of an application titled "NEGATIVE DIFFERENTIAL RESISTANCE (NDR) DEVICE AND METHOD OF OPERATING SAME" serial no. 10/315,741 filed December 10, 2002. The aforementioned serial no. 10/315,741 application claims priority to and is in turn a continuation of an application titled "CMOS PROCESS COMPATIBLE, TUNABLE NDR (NEGATIVE DIFFERENTIAL RESISTANCE) DEVICE AND METHOD OF OPERATING SAME," (serial no. 09/603,101 filed June 22, 2000, now U.S. patent 6,512,274).

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The present application is further related to and also claims priority to an application titled "CHARGE TRAPPING DEVICE AND METHOD FOR IMPLEMENTING A TRANSISTOR HAVING A NEGATIVE DIFFERENTIAL RESISTANCE MODE" (serial no. 09/603,102 filed June 22, 2000, now U.S. patent 6,479,862), and is further related to and claims priority to an application titled "CMOS COMPATIBLE PROCESS FOR MAKING A TUNABLE NEGATIVE DIFFERENTIAL RESISTANCE (NDR) DEVICE" (serial no. 09/602,658 filed June 22, 2000, now U.S. patent 6,596,617).

The above materials are expressly incorporated by reference herein.

FIELD OF THE INVENTION

This invention relates to semiconductor devices and more particularly to a CMOS compatible MIS device that exhibits negative differential resistance. The present invention is applicable to a wide range of semiconductor integrated circuits, particularly for high-density memory and logic applications, as well as power management applications.